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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/086,129	02/28/2002	David P. Schultz	X-1069 US	2232

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EXAMINER	
KERVEROS, JAMES C	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/086,129	SCHULTZ, DAVID P.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This is a FINAL Office Action in response to AMENDMENT filed 4/11/2005, in reply to the Office Action mailed 1/11/2005. Claims 1-27 are pending.

Prior art rejection is still maintained, as set forth in the last Office Action mailed 1/11/2005.

Claims 1-4 and 6–27 are rejected under 35 U.S.C. 102(e) as being anticipated by Nadeau-Dostie et al. (U.S. Patent 6,829,730). Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nadeau-Dostie et al. (U.S. Patent 6,829,730), as set forth in the present Office Action.

Response to Arguments

Applicant's arguments filed 4/11/2005 have been fully considered but they are not persuasive.

Regarding independent Claim 1, in response to Applicant's argument that Nadeau-Dostie fails to disclose a “selectable bit register" which extends "the apparent length of an instruction register of the host JTAG TAP controller", the Examiner notes that Nadeau-Dostie discloses a “selectable bit register", such as an (instruction register 125) comprising at least one available bit (in this case having five bits), which is selectable via multiplexer (132) and once selected it extends the apparent length of an instruction register (116) to a total of (eight bits) from the initial three bits, by combining

the five selected bits of instruction register 125 with the three bits of instruction register 116, Figure 3. Even though, instruction register 116 is shown to be physically outside of the TAP 100, functionally the register is controlled by TAP 100 via the Shift-IR command which controls (instruction register 125) via multiplexer (132) to be loaded into a TAP group. When an instruction is loaded into an instruction register, Shift-IR is active (Logic 1), which connect input 1 of multiplexer 132 to (instruction register 125), Figure 3.

Regarding independent Claim 7, in response to Applicant's argument that Nadeau-Dostie fails to disclose, "selecting an apparent register size based upon a number of IP cores implemented in the FpGA-based SoC.", Nadeau-Dostie discloses processor cores 18 and 20, Figure 1, having embedded TAPs, but may be part of any other core used to design complex circuits. The test data registers (not shown) of the TAPs can be used to control test and debug functions of the cores. The embedded TAPs are connected in a daisy-chain fashion, a configuration that is expected by many software development systems. Clearly, the extended register can be implemented with a TAP to control test and debug functions of a core.

Regarding independent Claim 11, in response to Applicant's argument that Nadeau-Dostie fails to disclose, a "selector for selecting said at least one available bit, the selector extending an apparent length of an instruction register of the host", it is noted that Nadeau-Dostie discloses multiplexer (132) which selects instruction register 125 and extends the apparent length of the instruction register (116) to a total of (eight bits) from the initial three bits.

Regarding independent Claim 14, in response to Applicant's argument that Nadeau-Dostie fails to disclose, an "instruction register size select signal enabling the selection of an apparent register size to accommodate a variable number IP cores", the Examiner notes that Nadeau-Dostie discloses an "instruction register size select signal" such as Shift-IR control signal to determine the source of the data loaded into a TAP group. When an instruction is loaded into an instruction register, Shift-IR is active (Logic 1), which connect input 1 of each of multiplexers 132 and 134 to their respective group TDI input, thus extending he register accordingly to accommodate testing of cores, Figures 1 and 3.

Regarding independent Claim 18, in response to Applicant's argument that Nadeau-Dostie fails to disclose the method steps recited in claim 18, the Examiner wishes to direct the Applicant to the Office Action in reference to claim 18 rejection.

Regarding independent Claim 21, in response to Applicant's argument that Nadeau-Dostie fails to disclose a system as recited in claim 21, it is noted that (Figure 1, Nadeau-Dostie) shows a typical arrangement of TAPs contained in a circuit 10, comprising a plurality of IP cores (18, 20) each including a JTAG TAP controller (eTAP1 14 and eTAP2 16). A host JTAG TAP controller (TAP 12, Master TAP) coupled to each of the JTAG TAP controllers 14 and 16, the host JTAG TAP controller 12 comprising a selectable bit register 125 for selecting an apparent length of an instruction register (116) from the initial three shift register elements to a total of (eight bits) by using the five selected bits from the selectable register 125, based upon a number of IP cores (18, 20) implemented in the circuit 10.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAMES C KERVEROS
Examiner
Art Unit 2133

By: _____.

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Date: 2 June 2005
Office Action: Final Rejection

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